AMENDMENTS TO THE CLAIMS:

1-10.   (Canceled).

11.   (Previously presented) A method for monitoring a main-clock generated by a main-microcomputer and a sub-clock, said sub-clock including a smaller number of clock pulses than those of said main-clock, said method comprising:

initializing said main-microcomputer at a time point during a specific period of time beginning when it is detected that said main-microcomputer has stopped supply of said main-clock; and

when it is confirmed that said main-microcomputer has not resumed supply of said main-clock during said specific period of time, outputting a switch signal to allow switching from said main-clock to said sub-clock.

12.   (Previously presented) The method according to claim 11, wherein said initializing comprises issuing an initializing signal synchronized with a clock pulse of said sub-clock, said clock pulse of said sub-clock occurring immediately after said detection that said main-microcomputer has stopped supply of said main-clock.

13.   (Previously presented) The method according to claim 11, wherein said specific period of time is determined by beginning to count a predetermined number of clock pulses of said sub-clock after an initializing signal is issued.

14.   (Previously presented) The method according to claim 11, further comprising:

after outputting said switch signal, when it is detected that said sub-clock is not supplied

any more, issuing a flag signal indicative that both said main-clock and sub-clock are not

supplied any more.

15.   (Previously presented) A clock monitoring method, comprising:

(a)   counting clock pulses of a main-clock generated by a main-microcomputer to

determine a first clock count indicative of how many clock pulses of said main-clock have been

counted during a predetermined period of time;

(b)   when said first clock count has reached a first threshold, determining said main-

microcomputer is in normal operation;

(c)   when said first clock count has not reached said first threshold, upon completion

of said determination of said first clock count, resetting said main-clock by issuing a reset signal

synchronized with a clock pulse of a sub-clock and immediately occurring after said completion

of said determination of said first clock count, said sub-clock containing a smaller number of

clock pulses than those of said main-clock, and simultaneously, counting clock pulses of said

sub-clock after said completion of said determination of said first clock count to determine a

second clock count indicative of how many clock pulses of said sub-clock have been counted

after resetting said main-clock;

(d)   when said first clock count has not reached said first threshold and said main-

microcomputer is restored before said second clock count reaches a second threshold,

determining said main-microcomputer has been restored to normal operations; and

(e)   when said first clock count has not reached said first threshold and said main-microcomputer is not restored before said second clock count reaches said second threshold, outputting a switch signal to allow switching from said main-clock to said sub-clock.

16.   (Previously presented) The method according to claim 15, further comprising after the step (e), when said sub-clock is not supplied any more, issuing a first flag signal indicative that both said main-clock and sub-clock are not supplied any more.

17.   (Previously presented) The method according to claim 15, wherein the step (b) further comprises:

issuing a second flag signal indicating said main-microcomputer is in normal operation.

18.   (Previously presented) The clock monitoring method according to claim 17, wherein the step (c) further comprises:

issuing a third flag signal having outputs corresponding to high and low levels of said second flag signal.

19.   (Previously presented) The method according to claim 18, wherein said second count is determined by counting clock pulses of an output signal beginning when said reset signal is issued, said output signal being created by calculating a logical sum of said sub-clock and said third flag signal.

20.   (Previously presented) The method according to claim 18, wherein the step (b) further

comprises:

      setting said second clock count to be zero using a fourth flag signal created by delaying

said third flag signal by a predetermined period to produce a new flag signal and then inverting

said new flag signal.

21.   (Previously presented) The method according to claim 20, wherein said first flag signal is

created so that said sub-clock is delayed a predetermined period to produce a first delay signal,

said first delay signal is delayed a predetermined period to produce a second delay signal, an

exclusive - OR of said sub-clock and said first and second delay signals is calculated, and said

first flag signal is determined by computing a logical product of said exclusive - OR and said

fourth flag signal.

22.   (Previously presented) A method of changing a clock signal from a main-clock supplied

by a data processor to a sub-clock, comprising:

      monitoring said main-clock to detect that said main-clock has stopped;

      initializing said data processor to attempt to restore said main-clock; and

      allowing said sub-clock to be supplied instead of said main-clock when said main-clock

is not restored during a specific period of time.

23.   (Previously presented) A method for monitoring a main-clock generated by a main-

microcomputer and a sub-clock, said method comprising:

      detecting whether said main-microcomputer has stopped supply of said main-clock;

initializing said main-microcomputer at a time point during a specific period of time

beginning when said detecting detects that said main-microcomputer has stopped supply of said

main-clock;

confirming whether said main-microcomputer has resumed supply of said main-clock

during said specific period of time; and

outputting a switch signal to switch from said main-clock to said sub-clock when said

confirming confirms that said main-microcomputer has not resumed supply of said main-clock

during said specific period of time,

wherein a number of clock pulses of said sub-clock is less than a number of clock pulses

of said main-clock.

24.   (Previously presented) The method according to claim 11, wherein, when it is confirmed

that said main-microcomputer has resumed supply of said main-clock during said specific period

of time, determining that said main-microcomputer has been restored to normal operations.

25.   (Previously presented) The method according to claim 24, further comprising issuing a

second flag signal indicating said main-microcomputer is in normal operation.

26.   (Previously presented) The method according to claim 11, wherein, when it is confirmed

that said main-microcomputer has resumed supply of said main-clock during said specific period

of time, determining that outputting a switch signal to switch from said main-clock to said sub-

clock is not necessary.

27.   (Previously presented) The method according to claim 11, wherein said initializing

comprises issuing an initializing signal synchronized with a clock pulse of said sub-clock.

28.   (Previously presented) The method according to claim 27, wherein said clock pulse of

said sub-clock occurs immediately after said detection that said main-microcomputer has stopped

supply of said main-clock.

29.   (New) The method according to claim 22, wherein said specific period of time is

determined by beginning to count a predetermined number of clock pulses of said sub-clock after

an initializing signal is issued.

30.   (New) The method according to claim 23, wherein said specific period of time is

determined by beginning to count a predetermined number of clock pulses of said sub-clock after

an initializing signal is issued.